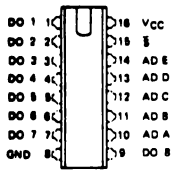
SCHOTTKY† PROM'S

SERIES 54S/74S PROGRAMMABLE READ-ONLY MEMORIES

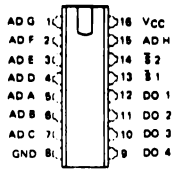
- Titanium-Tungsten (Ti-W) Fuse Links for Fast, Low-Voltage, Reliable Programming
- All Schottky-Clamped PROM's Offer:
  - Fast Chip Select to Simplify System Decode
  - Choice of Three-State or Open-Collector Outputs
  - P-N-P Inputs for Reduced Loading on System Buffers/Drivers
- Full Decoding and Chip Select Simplify System Design
- Applications Include:
  - Microprogramming/Firmware Loaders
  - Code Converters/Character Generators
  - Translators/Emulators
  - Address Mapping/Look-Up Tables

TYPE NUMBER (PACKAGES)		BIT SIZE (ORGANIZATION)	OUTPUT CONFIGURATION	TYPICAL PERFORMANCE	
−55°C to 125°C	0°C to 70°C			ADDRESS ACCESS TIME	POWER DISSIPATION
SN54S188(J, W)	SN74S188(J, N)	256 bits	open-collector	25 ns	400 mW
SN54S288(J, W)	SN74S288(J, N)	(32 W x 8 B)	three-state		
SN54S287(J, W)	SN74S287(J, N)	1024 bits	three-state	42 ns	500 mW
SN54S387(J, W)	SN74S387(J, N)	(256 W x 4 B)	open-collector		
SN54S470(J)	SN74S470(J, N)	2048 bits	open-collector	50 ns	550 mW
SN54S471(J)	SN74S471(J, N)	(256 W x 8 B)	three-state		
SN54S472(J)	SN74S472(J, N)	4096 bits	three-state	55 ns	600 mW
SN54S473(J)	SN74S473(J, N)	(512 W x 8 B)	open-collector		
SN54S474(J, W)	SN74S474(J, N)	4096 bits	three-state	55 ns	600 mW
SN54S475(J, W)	SN74S475(J, N)	(512 W x 8 B)	open-collector		

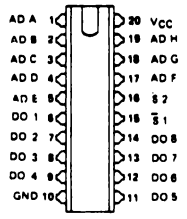
256 BITS (32 WORDS BY 8 BITS) '8188, '8288



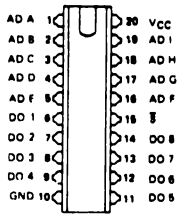
1024 BITS (256 WORDS BY 4 BITS) '8287, '8387



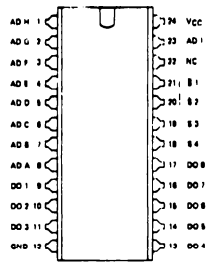
2048 BITS (256 WORDS BY 8 BITS) '8470, '8471



4096 BITS (512 WORDS BY 8 BITS) '8472, '8473



4096 BITS (512 WORDS BY 8 BITS) '8474, '8475



†Pin assignments for all of these memories are the same for all packages.

description

These monolithic TTL programmable read-only memories (PROM's) feature titanium-tungsten (Ti-W) fuse links with each link designed to program in one millisecond or less. These PROM's offer considerable flexibility for upgrading existing designs or improving new designs as they feature full Schottky clamping for improved performance, low-current MOS-compatible p-n-p inputs, choice of bus-driving three-state or open-collector outputs, and improved chip-select access times.

The high-complexity 2048- and 4096-bit 20-pin PROM's can be used to significantly improve system density for fixed memories as all are offered in a dual-in-line package having pin-row spacings of 0.300 inch.

description (continued)

Data can be electronically programmed, as desired, at any bit location in accordance with the programming procedure specified. All PROM's, except the 'S287 and 'S387, are supplied with a low-logic-level output condition stored at each bit location. The programming procedure open-circuits Ti-W metal links, which reverses the stored logic level at selected locations. The procedure is irreversible; once altered, the output for that bit location is permanently programmed. Outputs never having been altered may later be programmed to supply the opposite output level. Operation of the unit within the recommended operating conditions will not alter the memory content.

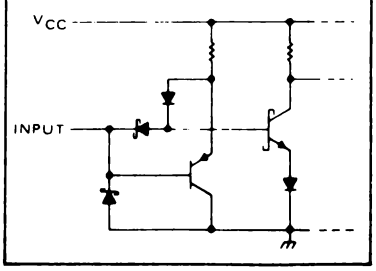
Active level(s) at the chip-select input(s) enables all of the outputs. An inactive level at any chip-select input causes all outputs to be off.

The three-state output offers the convenience of an open-collector output with the speed of a totem-pole output; it can be bus-connected to other similar outputs yet it retains the fast rise time characteristic of the TTL totem-pole output. The open-collector output offers the capability of direct interface with a data line having a passive pull-up.

schematics of inputs and outputs

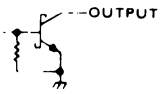
'S188, 'S287, 'S288, 'S387, 'S470, 'S471, 'S472, 'S473, 'S474, 'S475

EQUIVALENT OF EACH INPUT



'S188, 'S387, 'S470, 'S473, 'S475

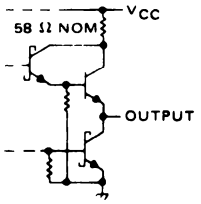
TYPICAL OF ALL OUTPUTS



Programming circuit not shown

'S287, 'S288, 'S471, 'S472, 'S474

TYPICAL OF ALL OUTPUTS



Programming circuit not shown

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S' Circuits . . . . . −55°C to 125°C
SN74S' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended conditions for programming

		SN54S', SN74S'			UNIT
		MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	Steady state	4.75	5	5.75	V
	Program pulse	10	10.5	11†	
Input voltage	High level, V_{IH}	2.4		5	V
	Low level, V_{IL}	0		0.5	
Termination of all outputs except the one to be programmed		See load circuit (Figure 1)			
Voltage applied to output to be programmed, $V_{O(pr)}$ (see Note 2)		0	0.25	0.3	V
Duration of V_{CC} programming pulse Y (see Figure 2 and Note 3)		0.9	1	10	ms
Programming duty cycle			25	35	%
Free-air temperature		0		55	°C

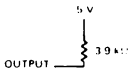
†Absolute maximum ratings.

NOTES: 1. Voltage values are with respect to network ground terminal. The supply-voltage rating does not apply during programming.
2. The 'S188, 'S288, 'S470, 'S471, 'S472, 'S473, 'S474, and 'S475 are supplied with all bit locations containing a low logic level, and programming a bit changes the output of the bit to high logic level. The 'S287 and 'S387 are supplied with all bit outputs at a high logic level, and programming a bit changes it to a low logic level.
3. Programming is guaranteed if the pulse applied is 0.9 ms long.

step-by-step programming procedure

1. Apply steady-state supply voltage (V_{CC} = 5 V) and address the word to be programmed.
2. Verify that the bit location needs to be programmed. If not, proceed to the next bit.
3. If the bit requires programming, disable the outputs by applying a high-logic-level voltage to the chip-select input(s).
4. Only one bit location is programmed at a time. Connect each output not being programmed to 5 V through 3.9 kΩ and apply the voltage specified in the table to the output to be programmed. Maximum current out of the programming output supply during programming is 150 mA.
5. Step V_{CC} to 10.5 V nominal. Maximum supply current required during programming is 750 mA.
6. Apply a low-logic-level voltage to the chip-select input(s). This should occur between 10 μs and 1 ms after V_{CC} has reached its 10.5-V level. See programming sequence of Figure 2.
7. After the X pulse time (1 ms) is reached, a high logic level is applied to the chip-select inputs to disable the outputs.
8. Within 10 μs to 1 ms after the chip-select input(s) reach a high logic level, V_{CC} should be stepped down to 5 V at which level verification can be accomplished.
9. The chip-select input(s) may be taken to a low logic level (to permit program verification) 10 μs or more after V_{CC} reaches its steady-state value of 5 V.
10. At a Y pulse duty cycle of 35% or less, repeat steps 1 through 8 for each output where it is desired to program a bit.

NOTE: Only one programming attempt per bit is recommended.



LOAD CIRCUIT FOR EACH OUTPUT NOT BEING PROGRAMMED OR FOR PROGRAM VERIFICATION
FIGURE 1

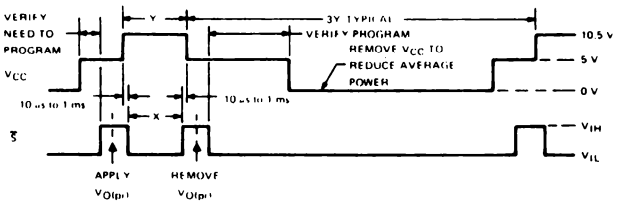


FIGURE 2–VOLTAGE WAVEFORMS FOR PROGRAMMING

recommended operating conditions

		'S287, 'S471			'S288			'S472, 'S474			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	Series 54S	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	Series 74S	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	Series 54S			−2			−2			−2	mA
	Series 74S			−6.5			−6.5			−6.5	
Low-level output current, I_{OL}				16			20			12	mA
Operating free-air temperature, T_A	Series 54S	−55		125♦	−55		125	−55		125	°C
	Series 74S	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54S'			SN74S'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = MAX	2.4	3.4		2.4	3.2		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.5			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_O = 2.4 V	V_{IH} = 2 V,			50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_O = 0.5 V	V_{IH} = 2 V,			−50			−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V			−250			−250	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−100	−30		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, Chip select(s) at 0 V, Outputs open, See Note 4	'S287		100	135		100	135	mA
			'S288		80	110		80	110	
			'S471		110	155		110	155	
			'S472, 'S474		120	155		120	155	

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE	TEST CONDITIONS	$t_{a(ad)}$ (ns) Access time from address		$t_{a(\overline{S})}$ (ns) Access time from chip select (enable time)		t_{PXZ} (ns) Disable time from high or low level	
		TYP‡	MAX	TYP‡	MAX	TYP‡	MAX
SN54S287	C_L = 30 pF for $t_{a(ad)}$ and $t_{a(\overline{S})}$ 5 pF for t_{PXZ}; R_L = 300 Ω; See Figure 4	42	75	15	40	12	40
SN74S287		42	65	15	35	12	35
SN54S288		25	50	12	30	8	30
SN74S288		25	40	12	25	8	20
SN54S471		50	80	20	40	15	35
SN74S471		50	70	20	35	15	30
SN54S472, SN54S474		55	85	20	45	15	40
SN74S472, SN74S474		55	75	20	40	15	35

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
♦An SN54S287 in the W package operating at free-air temperatures above 108°C requires a heat sink that provides a thermal resistance from case-to-free-air, $R_{\theta CA}$, of not more than 42°C/W.
NOTE 4: The typical values of I_{CC} shown are with all outputs low.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

recommended operating conditions

		'188			'387, '470			'473, '475			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	Series 54S	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	Series 74S	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output voltage, V_{OH}				5.5			5.5			5.5	V
Low-level output current, I_{OL}				20			16			12	mA
Operating free-air temperature, T_A	Series 54S	−55		125	−55		125♦	−55		125	°C
	Series 74S	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

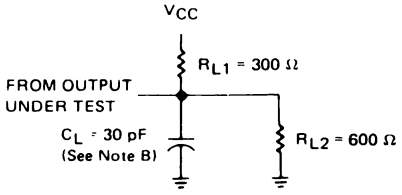
PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.2	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	V_{OH} = 2.4 V			50	μA
			V_{OH} = 5.5 V			100	
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V			−250	μA
I_{CC}	Supply current	V_{CC} = MAX, Chip select(s) at 0 V, Outputs open, See Note 4	'188		80	110	mA
			'387		100	135	
			'470		110	155	
			'473; '475		120	155	

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

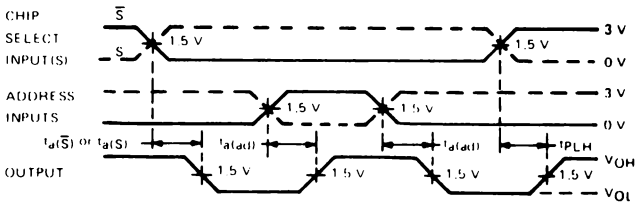
TYPE	TEST CONDITIONS	$t_{a(ad)}$ (ns) Access time from address		$t_{a(\overline{S})}$ (ns) Access time from chip select (enable time)		t_{PLH} (ns) Propagation delay time, low-to-high-level output from chip select (disable time)	
		TYP‡	MAX	TYP‡	MAX	TYP‡	MAX
SN54S188	C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω, See Figure 3	25	50	12	30	12	30
SN74S188		25	40	12	25	12	25
SN54S387		42	75	15	40	15	40
SN74S387		42	65	15	35	15	35
SN54S470		50	80	20	40	15	35
SN74S470		50	70	20	35	15	30
SN54S473, SN54S475		55	85	20	45	15	40
SN74S473, SN74S475		55	75	20	40	15	35

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
♦An SN54S387 in the W package operating at free-air temperatures above 108°C requires a heat sink that provides a thermal resistance from case-to-free-air, $R_{\theta CA}$, of not more than 42°C/W.
NOTE 4: The typical values of I_{CC} shown are with all outputs low.

PARAMETER MEASUREMENT INFORMATION



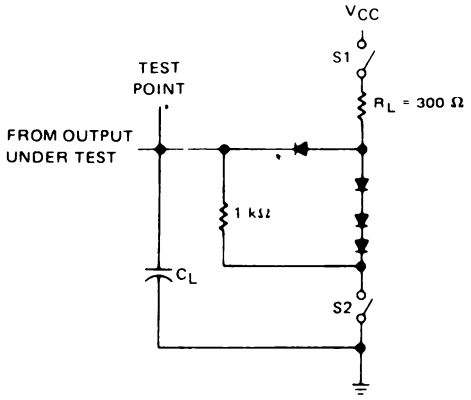
LOAD CIRCUIT



VOLTAGE WAVEFORMS

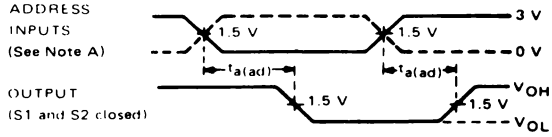
NOTES:
A. The input pulse generator has the following characteristics: $Z_{out} \approx 50\ \Omega$, PRR ≤ 1 MHz, $t_r \leq 2.5$ ns, and $t_f \leq 2.5$ ns.
B. C_L includes probe and jig capacitance.
C. The pulse generator is connected to the input under test. The other inputs, memory content permitting, are connected so that the input will switch the output under test.

FIGURE 3 – SWITCHING TIMES OF 'S188, 'S470, 'S387, 'S473, AND 'S475

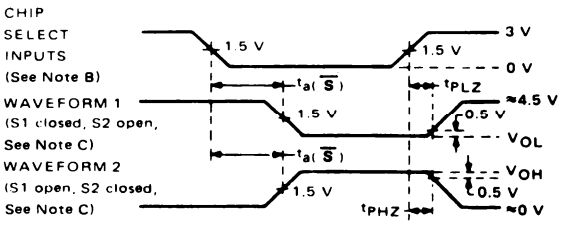


C_L includes probe and jig capacitance.
All diodes are 1N3064.

LOAD CIRCUIT



ACCESS TIME FROM ADDRESS INPUTS VOLTAGE WAVEFORMS



$t_{PXZ} = t_{PHZ}$ or t_{PLZ}

ACCESS (ENABLE) TIME AND DISABLE TIME FROM CHIP SELECT VOLTAGE WAVEFORMS

NOTES: A. When measuring access times from address inputs, the chip-select input(s) is(are) low.
B. When measuring access and disable times from chip-select input(s), the address inputs are steady-state.
C. Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.
D. Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz, and $Z_{out} \approx 50\ \Omega$.

FIGURE 4 – SWITCHING TIMES OF 'S287, 'S288, 'S471, 'S472, AND 'S474

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222